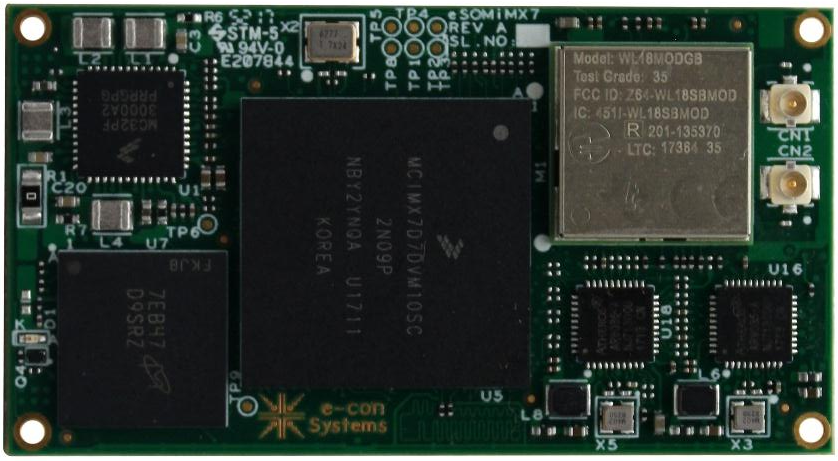
eSOMiMX7

Datasheet



Version 1.3

e-con Systems

5/8/2018

e-con Systems

Your Product Development Partner

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Contents

Introduction to eSOMiMX7

e-con Systems has developed an ultra-low power Computer-On-Module/System-On-Module eSOMiMX7, based on NXP® i.MX 7 embedded System on Chip (SoC) with the basic peripherals in a compact form factor. The SoC features a single or dual-core ARM® Cortex® A7 processor with an additional ARM Cortex M4 processor. The eSOMiMX7 has iMX7 CPU running up to 1 GHz – Dual/Solo Core, LPDDR3-1066 SDRAM configurable up to 2 GB and eMMC configurable up to 32 GB (Only for Dual Core) or a NAND Flash configurable up to 4 GB. The eSOMiMX7 module also has the Wireless LAN and Bluetooth module.

As part of the Productized Services program of e-con Systems, the eSOMiMX7 is aimed at reducing the time-to-market for our customers by making use of the stabilized and ready-to-market eSOMiMX7 modules in the customer applications. Being offered in a compact form factored modules with various configurations and OS support, these modules will enable our customers to focus on their application design.

This eSOMiMX7 is powered by Linux. The SOM is targeted to customers to reduce the Time-to-Market, by not worrying about the CPU subsystem, but to focus on the application base board design. This enables customers to build variety of base boards targeting various applications with a host of peripherals and interfaces.

The module delivers state of the art technology, targeting low power systems that still require high CPU performance. It also offers all the interfaces needed in a modern embedded device. It offers a wide range of interfaces from simple GPIOs, industry standard I2C, SPI, CAN, and UART buses to high-speed USB 2.0 interfaces. Besides the internal Flash Memory, there are several interfaces available for data storage such as SD memory card and eMMC storage. The CPU board also exposes the complete range of interfaces provided by the iMX7 application processor through its connectors so that the customers can access the complete functionality.

e-con Systems has a base board named ACACIA built around eSOMiMX7 for evaluation. The ACACIA base board will be available for customers with complete source code and other design inputs such as schematics, DXF and so on. The complete features of eSOMiMX7 and the variety of add-on modules supported by e-con Systems are available on our website www.e-consystems.com.

Please write to sales@e-consystems.com to get the specific details of eSOMiMX7.

The scope of this document includes technical details of the module from the hardware design perspective. This document will serve as a single point of reference for hardware design of the customer application using eSOMiMX7. This will provide the necessary details for the customers to integrate our eSOMiMX7 with their application board design. The schematic designer and layout designer would find this document very useful.

1 Features Summary

The features of iMX7 are described in this section.

1.1 CPU

- NXP's i.MX7 Solo ARM™ Cortex-A7 based CPU @ 800 MHz and Cortex-M4 Core @ 200 Mhz.

Or

- NXP's i.MX7 Dual ARM™ Cortex-A7 based CPU @ 1 GHz and Cortex-M4 Core @ 200 Mhz.

1.2 Memory

- LPDDR3-1066 x32-Bit (Expandable up to 2 GB)
- eMMC FLASH Expandable up to 64 GB (Only for Dual Core SOM) or NAND Flash (Expandable up to 4 GB)

1.3 Connector Interfaces – 100 Pins

- USB OTG 2.0 (x1)
- 24-bit Parallel LCD lines(x1)
- Gigabit Ethernet through On-SOM Gigabit Ethernet PHY (x1)
- SD/MMC (4bit) (x1)
- I2C (x4)
- SPI (x2)
- QSPI (x2)
- FlexCAN (x2)
- PWM (x3)
- UART (x2) (with CTS and RTS) (x5)
- MIPI-DSI (x1)
- MIPI CSI (x1)
- ADC (8 channels)
- SAI (x1)
- GPIOs

1.4 eSOMiMX7 Dual Specific Interfaces

- PCIe Gen 2.0 (x1)
- USB OTG 2.0 (x1)
- EPDC (x1)
- SAI (x1)[1]
- Gigabit Ethernet through On-SOM Gigabit Ethernet PHY (x1)[2]

These interfaces are in addition to the connector interfaces mentioned.

[1] First SAI Interface cannot be used when NAND is used.

[2] Second Ethernet cannot be used when EPDC is used.

1.5 General Specification

- Power Supply: 3.3V
- Temperature:
  - -20 to 85 degrees Celsius (Extended)
  - 0 to 70 degrees Celsius (Commercial)
- Form Factor: 55mm X 30mm

Block Diagram of eSOMiMX7

This section describes the main hardware blocks of eSOMiMX7.

2 Block Diagram of eSOMiMX7

The following figure shows the block diagram of eSOMiMX7.

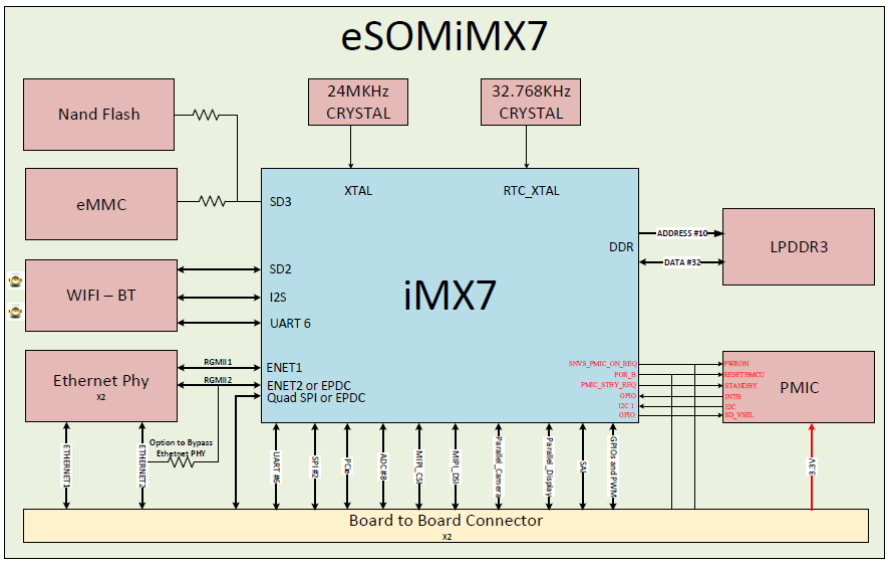

Figure 1: Block Diagram of eSOMiMX7

The main hardware blocks of eSOMiMX7 are as follows:

- NXP i.MX7 CPU
- On Board Memory
- Dual 10/100/1Gbps Ethernet PHY Transceiver
- Wi-Fi + Bluetooth Combo

The following sections describe each of the main hardware blocks in detail.

2.1 NXP i.MX7 CPU

eSOMiMX7 is based on NXP's i.MX7 Dual/Solo ARM™ Cortex-A7 core-based CPU which can operate up to 1 GHz speed per core in the case of Dual core and up to 800 MHz in the case of Solo core.

For more information about the features, please refer to the following documents from NXP:

- *iMX7 Datasheet*
- *User Manual*
- *Application Notes*

2.2 On Board Memory

The on-board memory types available in eSOMiMX7 are as follows:

- LPDDR3 SDRAM
- eMMC or NAND Flash – storage

2.2.1 LPDDR3 SDRAM

eSOMiMX7 supports the on-board memory of up to 2 GB. The iMX7 LPDDR3 interfaces up to 32-bits wide and operates at 533 MHz clock frequency.

2.2.2 eMMC or NAND Flash – Storage

eSOMiMX7 is available with 4GB of eMMC memory. This memory can be used for porting OS image that is user defined storage and expandable up to 64 GB.

Note: Only the Dual core version supports eMMC.

eSOMiMX7 is available with NAND Flash as an alternate to the eMMC in the Solo version of the SOM. NAND Flash can be expandable up to 4 GB.

2.3 10/100/1Gbps Ethernet PHY Transceiver

eSOMiMX7 features two gigabit Ethernet PHY. eSOMiMX7 can support (10Base-T/100Base-TX/1000Base-T) for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

Note: Solo processor and Dual core processor with EPDC interface will support only one Ethernet interface.

2.4 Wi-Fi and Bluetooth Combo

eSOMiMX7 contains Wi-Fi and Bluetooth module with the following features:

- IEEE STD 802.11a/b/g/n
- Bluetooth 4.1 and CSA2 Support
- Dual-Mode Bluetooth and BLE

eSOMiMX7 Ordering Information

This section describes about the eSOMiMX7 ordering information.

3 eSOMiMX7 Ordering Information

The ordering information of eSOMiMX7 for the following part number template is shown below.

Part Number Template: eSOMiMX7-Cx-N/Fxxx-Rxxx-WB-Ex-Fx-SWxx-ET

The following table lists the ordering information of eSOMiMX7.

Table 1: eSOMiMX7 Ordering Information

Feature	Options	P/N code	Notes
CPU	i.MX7 Solo Core 800 MHz	CS	
	i.MX7 Dual Core 1GHz	CD	
DDR SIZE	512MB	R512	
	1 GB	R1G	
	2 GB	R2G	
Storage	eMMC 4GB	F4G	Only for Dual
	eMMC 8GB	F8G	
	eMMC 16GB	F16G	
	eMMC 32GB	F32G	
	eMMC 64GB	F64G	
	NAND 512MB	N512	
	NAND 1GB	N1G	
	NAND 2GB	N2G	
	NAND 4GB	N4G	
Wi-Fi/BT	Not Present	-	
	Wi-Fi 802.11 b/g/n and Bluetooth 4.1	WB	
Ethernet Port	Not Present	-	
	Ethernet 1	SE	
	Ethernet 2	DE	Only for Dual
Fuse to Boot	Fuse to boot from eMMC	FE	Only for Dual
	Fuse to boot from SD	FS	
	Fuse to boot from NAND	FN	
	Not Fused	-	
Firmware version	Firmware version to be loaded into eMMC	SWxx	SWxx
	(xx – Running number starts from 01)		
Temperature	Extended Temperature	ET	-20C to 85C
	Commercial	-	0C to 70C

eSOMiMX7 Connector and Pin Mux

This section describes about the eSOMiMX7 connector pin-out.

eSOMiMX7 exposes two 100 pin connectors. The recommended mating connector for the interface is as follows:

- Manufacturer Part Number: DF40HC(3.0)-100DS-0.4V (51)
- Manufacturer: Hirose Electric Co Ltd

The following table lists the connector pin-out Table Header.

Table 2: Connector Pin-Out Table Header Description

Table Header	Description
Pin Number	This field represents connector number and pin number on the 100-pin board to board connector.
Pin Name	This item represents the signal name of the eSOMiMX7 two 100 pin connector.
IO Voltage	This field represents signal IO voltage.

4 eSOMiMX7 Connector Pin-Out

The pin number increases linearly with even numbers on one side and odd numbers on the other side of each connector. The following figure shows the bottom view of the eSOMiMX7 connector pin-out.

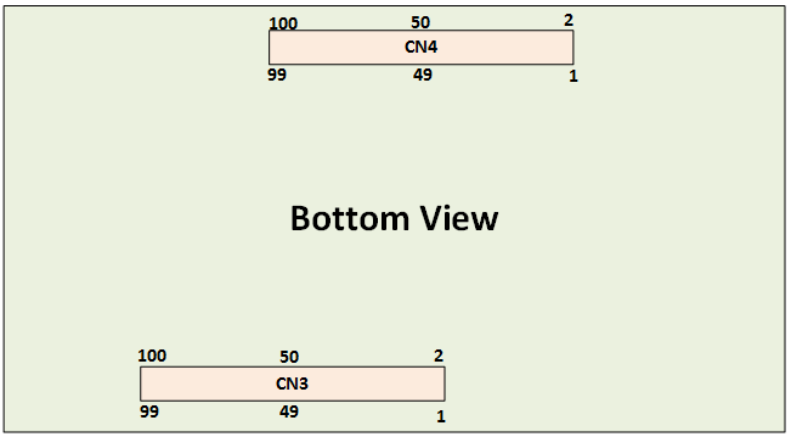

Figure 2: eSOMiMX7 Connector Pin-Out Bottom View

The following table lists the CN3 100 Pin-Out Details of eSOMiMX7.

Table 3: eSOMiMX7 CN3 100 Pin-Out Details

Pin #	Pin Name	IO Voltage	Note
CN3.1	iMX7_CONN_QSPI_A_DATA0	3.3V	
CN3.2	iMX7_CONN_QSPI_B_DATA0	3.3V	
CN3.3	iMX7_CONN_QSPI_A_DATA3	3.3V	
CN3.4	iMX7_CONN_QSPI_B_SS0_B	3.3V	
CN3.5	iMX7_CONN_QSPI_A_DATA1	3.3V	
CN3.6	iMX7_CONN_QSPI_B_DQS	3.3V	
CN3.7	iMX7_CONN_QSPI_A_SS0_B	3.3V	
CN3.8	iMX7_CONN_QSPI_B_DATA1	3.3V	
CN3.9	iMX7_CONN_QSPI_A_DATA2	3.3V	
CN3.10	iMX7_CONN_QSPI_B_DATA2	3.3V	
CN3.11	iMX7_CONN_QSPI_A_DQS	3.3V	
CN3.12	iMX7_CONN_QSPI_B_SS1_B	3.3V	
CN3.13	iMX7_CONN_QSPI_A_SCLK	3.3V	
CN3.14	iMX7_CONN_QSPI_B_DATA3	3.3V	
CN3.15	iMX7_CONN_QSPI_A_SS1_B	3.3V	
CN3.16	iMX7_CONN_QSPI_B_SCLK	3.3V	
CN3.17	GND	0V	
CN3.18	ETHERNET_P2_ACT	3.3V	Can be used as both active low and active high signal, please refer to the eSOMiMX7_Carrier_Board_Design_Guide for further details.
CN3.19	iMX7_CONN_EPDC_PWRCOM	3.3V	
CN3.20	ETHERNET_P2_LED_1000M	3.3V	Can be used as both active low and active high signal, please refer to the *eSOMiMX7_Carrier_Board_Design_Guide* for further details.
CN3.21	iMX7_CONN_EPDC_PWRSTAT	3.3V	
CN3.22	ETHERNET_P2_LED_100M	3.3V	Can be used as both active low and active high signal, please refer to the *eSOMiMX7_Carrier_Board_Design_Guide* for further details.
CN3.23	iMX7_CONN_EPDC_BDR1	3.3V	
CN3.24	CONN_RGMII2_RXD3	3.3V	
CN3.25	iMX7_CONN_EPDC_BDR0	3.3V	
CN3.26	GND	0V	
CN3.27	iMX7_LCD_ENABLE	1.8V	
CN3.28	CLK_iMX7_LCD_CLK	1.8V	
CN3.29	iMX7_LCD_DATA11	1.8V	
CN3.30	GND	0V	
CN3.31	iMX7_LCD_DATA17	1.8V	
CN3.32	iMX7_LCD_DATA12	1.8V	
CN3.33	iMX7_LCD_DATA23	1.8V	

CN3.34	iMX7_LCD_DATA8	1.8V	
CN3.35	iMX7_LCD_DATA7	1.8V	
CN3.36	iMX7_LCD_DATA0	1.8V	
CN3.37	GND	0V	
CN3.38	iMX7_LCD_DATA4	1.8V	
CN3.39	iMX7_LCD_HSYNC	1.8V	
CN3.40	iMX7_LCD_DATA2	1.8V	
CN3.41	iMX7_LCD_VSYNC	1.8V	
CN3.42	iMX7_LCD_DATA15	1.8V	
CN3.43	iMX7_LCD_DATA14	1.8V	
CN3.44	GND	0V	
CN3.45	iMX7_LCD_DATA9	1.8V	
CN3.46	iMX7_LCD_DATA18	1.8V	
CN3.47	iMX7_LCD_DATA22	1.8V	
CN3.48	iMX7_LCD_DATA13	1.8V	
CN3.49	iMX7_LCD_DATA10	1.8V	
CN3.50	iMX7_LCD_DATA21	1.8V	
CN3.51	iMX7_LCD_DATA20	1.8V	
CN3.52	iMX7_LCD_DATA19	1.8V	
CN3.53	iMX7_LCD_DATA5	1.8V	
CN3.54	iMX7_LCD_DATA1	1.8V	
CN3.55	iMX7_LCD_DATA6	1.8V	
CN3.56	iMX7_LCD_DATA16	1.8V	
CN3.57	iMX7_LCD_DATA3	1.8V	
CN3.58	iMX7_LCD_RESET	1.8V	
CN3.59	GND	0V	
CN3.60	GND	0V	
CN3.61	MIPI_DSI_D0_P_IMX7_CONN		
CN3.62	MIPI_CSI_D0_P_IMX7_CONN		
CN3.63	MIPI_DSI_D0_N_IMX7_CONN		
CN3.64	MIPI_CSI_D0_N_IMX7_CONN		
CN3.65	GND	0V	
CN3.66	GND	0V	
CN3.67	MIPI_DSI_CLK_P_IMX7_CON N		
CN3.68	MIPI_CSI_CLK_P_IMX7_CONN		
CN3.69	MIPI_DSI_CLK_N_IMX7_CON N		
CN3.70	MIPI_CSI_CLK_N_IMX7_CON N		
CN3.71	GND	0V	
CN3.72	GND	0V	
CN3.73	MIPI_DSI_D1_P_IMX7_CONN		
CN3.74	MIPI_CSI_D1_P_IMX7_CONN		
CN3.75	MIPI_DSI_D1_N_IMX7_CONN		
CN3.76	MIPI_CSI_D1_N_IMX7_CONN		
CN3.77	GND	0V	
CN3.78	GND	0V	
CN3.79	P1MDIDN		

CN3.80	P2MDIBN	3.3V	Internally muxed with EPDC signals.
CN3.81	P1MDIDP		
CN3.82	P2MDIBP	3.3V	Internally muxed with EPDC signals.
CN3.83	GND	0V	
CN3.84	GND	0V	
CN3.85	P1MDIBN		
CN3.86	P2MDIAP	3.3V	Internally muxed with EPDC signals.
CN3.87	P1MDIBP		
CN3.88	P2MDIAN	3.3V	Internally muxed with EPDC signals.
CN3.89	GND	0V	
CN3.90	GND	0V	
CN3.91	P1MDICN		
CN3.92	P2MDICP	3.3V	Internally muxed with EPDC signals.
CN3.93	P1MDICP		
CN3.94	P2MDICN	3.3V	Internally muxed with EPDC signals.
CN3.95	GND	0V	
CN3.96	GND	0V	
CN3.97	P1MDIAN		
CN3.98	P2MDIDP	3.3V	Internally muxed with EPDC signals.
CN3.99	P1MDIAP		
CN3.100	P2MDIDN	3.3V	Internally muxed with EPDC signals.

The following table lists the CN4 100 Pin-Out Details of eSOMiMX7.

Table 4: eSOMiMX7 CN4 100 Pin-Out Details

Pin #	Pin Name	IO Voltage	Note
CN4.1	VCC_LICELL		
CN4.2	VCC_3P3_IN	3.3V	
CN4.3	GND	0V	
CN4.4	VCC_3P3_IN	3.3V	
CN4.5	PCIe_RX_N_iMX7_CONN		An external series capacitor is recommended.
CN4.6	VCC_3P3_IN	3.3V	
CN4.7	PCIe_RX_P_iMX7_CONN		An external series capacitor is recommended.
CN4.8	VCC_3P3_IN	3.3V	
CN4.9	GND	0V	
CN4.10	VCC_3P3_IN	3.3V	
CN4.11	PCIe_TX_N_iMX7_CONN		An external series capacitor is recommended.
CN4.12	VCC_3P3_IN	3.3V	

CN4.13	PCIe_TX_P_iMX7_CONN		An external series capacitor is recommended.
CN4.14	VCC_3P3_IN	3.3V	
CN4.15	GND	0V	
CN4.16	VCC_3P3_IN	3.3V	
CN4.17	CLK_PCIe_CLK_N_iMX7_CONN		A parallel termination is recommended.
CN4.18	VCC_3P3_IN	3.3V	
CN4.19	CLK_PCIe_CLK_P_iMX7_CONN		A parallel termination is recommended.
CN4.20	VCC_3P3_IN	3.3V	
CN4.21	GND	0V	
CN4.22	VCC_3P3_IN	3.3V	
CN4.23	iMX7_CONN_TAMPER2	SNVS	
CN4.24	GND	0V	
CN4.25	iMX7_CONN_TAMPER1	SNVS	
CN4.26	ADC1_IN2_IMX7_CONN	1.8V	
CN4.27	iMX7_CONN_TAMPER0	SNVS	
CN4.28	ADC1_IN0_IMX7_CONN	1.8V	
CN4.29	VDD_SNVS_1P8_CAP	SNVS	
CN4.30	ADC1_IN3_IMX7_CONN	1.8V	
CN4.31	CPU_ONOFF	SNVS	Internally pulled up to SNVS Voltage.
CN4.32	ADC1_IN1_IMX7_CONN	1.8V	
CN4.33	CPU_POR	SNVS	Internally pulled up to SNVS Voltage. Please refer to the CPU Power and Reset, for more details.
CN4.34	ADC2_IN0_IMX7_CONN	1.8V	
CN4.35	CPU_BOOT_MODE1	1.8V	Internally pulled up to 1.8V.
CN4.36	ADC2_IN1_IMX7_CONN	1.8V	
CN4.37	CPU_BOOT_MODE0	1.8V	Internally pulled up to 1.8V.
CN4.38	ADC2_IN2_IMX7_CONN	1.8V	
CN4.39	GPIO1_IO13_IMX7_CONN	1.8V	
CN4.40	ADC2_IN3_IMX7_CONN	1.8V	
CN4.41	GPIO1_IO12_IMX7_CONN	1.8V	
CN4.42	GND	0V	
CN4.43	GPIO1_IO10_IMX7_CONN	1.8V	
CN4.44	SAI1_TXD_iMX7_CONN	3.3V	Internally muxed with NAND flash.
CN4.45	GPIO1_IO09_IMX7_CONN	1.8V	
CN4.46	SAI1_RXD_iMX7_CONN	3.3V	Internally muxed with NAND flash.
CN4.47	GPIO1_IO07_IMX7_CONN	1.8V	
CN4.48	SAI1_TXC_iMX7_CONN	3.3V	Internally muxed with NAND flash.
CN4.49	GPIO1_IO06_IMX7_CONN	1.8V	
CN4.50	SAI1_RXFS_iMX7_CONN	3.3V	
CN4.51	GPIO1_IO04_IMX7_CONN	1.8V	
CN4.52	SAI1_RXC_iMX7_CONN	3.3V	

CN4.53	GPIO1_IO00_IMX7_CONN	1.8V	
CN4.54	SAI1_TXFS_iMX7_CONN	3.3V	Internally muxed with NAND flash.
CN4.55	GPIO1_IO02_IMX7_CONN	1.8V	
CN4.56	GND	0V	
CN4.57	GND	0V	
CN4.58	CLK_SAI1_MCLK_iMX7_CONN	3.3V	Internally muxed with NAND flash.
CN4.59	I2C4_DATA_IMX7_CONN	1.8V	An external 1.8V pull up is recommended.
CN4.60	GND	0V	
CN4.61	I2C4_CLK_IMX7_CONN	1.8V	An external 1.8V pull up is recommended.
CN4.62	UART3_RX_IMX7_CONN	1.8V	
CN4.63	I2C2_DATA_IMX7_CONN	1.8V	An external 1.8V pull up is recommended.
CN4.64	UART1_RX_IMX7_CONN	1.8V	
CN4.65	I2C2_CLK_IMX7_CONN	1.8V	An external 1.8V pull up is recommended.
CN4.66	UART2_RX_IMX7_CONN	1.8V	
CN4.67	I2C3_DATA_IMX7_CONN	1.8V	An external 1.8V pull up is recommended.
CN4.68	UART1_TX_IMX7_CONN	1.8V	
CN4.69	I2C3_CLK_IMX7_CONN	1.8V	An external 1.8V pull up is recommended.
CN4.70	ETHERNET_P1_LED_1000M		
CN4.71	SAI2_FS_iMX7_CONN	3.3V	
CN4.72	ETHERNET_P1_LED_1000M		
CN4.73	SAI2_RXD_iMX7_CONN	3.3V	
CN4.74	ETHERNET_P1_LED_100M		
CN4.75	SAI2_TXD_iMX7_CONN	3.3V	
CN4.76	VBUS_USB_OTG1	5V	
CN4.77	SAI2_TXC_iMX7_CONN	3.3V	
CN4.78	USB_OTG1_ID_iMX7_CONN	3.3V	
CN4.79	GND	0V	
CN4.80	USB_OTG2_ID_iMX7_CONN	3.3V	
CN4.81	CLK_SD1_CLK_iMX7_CONN		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.82	VBUS_USB_OTG2	5V	
CN4.83	GND	0V	
CN4.84	GND	0V	
CN4.85	SD1_DATA3_iMX7_CONN	3.3V	IO Voltage is 1.8V/3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.86	USB_OTG1_DP_iMX7_CONN		
CN4.87	SD1_DATA1_iMX7_CONN		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.88	USB_OTG1_DN_iMX7_CONN		

CN4.89	SD1_DATA2_iMX7_CONN		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.90	GND	0V	
CN4.91	SD1_CMD_iMX7_CONN		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.92	USB_OTG2_DP_iMX7_CONN		
CN4.93	SD1_DATA0_iMX7_CONN		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.94	USB_OTG2_DN_iMX7_CONN		
CN4.95	nSD1_CD_iMX7_CONN		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.96	GND	0V	
CN4.97	VCC_SD		IO Voltage is 1.8V /3.3V. Please refer to the MMC or SD Interface section, for more details.
CN4.98	NC		Must be left unconnected.
CN4.99	VCC_1P8		
CN4.100	NC		Must be left unconnected.

This section describes the various interfaces terminated in the connectors by referring to the default pin names. However, many additional interface options are available when different modes are selected.

5 Peripheral Interfaces

The following table lists the interfaces table header description.

Table 5: Interfaces Table Header Description

Table Header	Description
Pin Number	This item represents the pin number on the two 100-pin board to board connector.
Pin Name	This item represents the Signal Name of the eSOMiMX7 connector. The Signal Name is abbreviation of the signal functionality.
Pin Type	This field explains the I/O type of the signal. The values are explained as: I: Digital CMOS input O: Digital CMOS output IO: Digital CMOS Bidirectional Input/output PU/PD: Pull up / down on signal DS: Differential signal P: Power supply or Ground pin
IO Voltage	Pin functionality description.

5.1 Display Subsystem

The display subsystem consists of the following display interfaces:

- MIPI DSI
- Parallel Display – 24 Bits
- Electrophoretic Display

5.1.1 MIPI DSI

MIPI DSI interface supports the following features:

- Compliant with MIPI Alliance specification for Display Serial Interface (DSI), Version V1.01r11.
- Fully Compliant with MIPI Alliance standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Supports up to 2 D-PHY Data Lanes
  - Maximum resolution: up to SXGA+(1400 x 11050 @ 60 Hz, 24 bpp)
  - Video Mode Pixel Formats, 16 bpp, 18 bpp packed, 18 bpp loosely packed (3-byte format), and 24bpp.

The following table lists the MIPI DSI signal details.

Table 6: MIPI DSI Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.61	MIPI_DSI_D0_P_IMX7_CONN	DS	Positive DSI data 0 differential
CN3.63	MIPI_DSI_D0_N_IMX7_CONN	DS	Negative DSI data 0 differential
CN3.67	MIPI_DSI_CLK_P_IMX7_CONN	DS	Positive DSI clock differential
CN3.69	MIPI_DSI_CLK_N_IMX7_CONN	DS	Negative DSI clock differential
CN3.73	MIPI_DSI_D1_P_IMX7_CONN	DS	Positive DSI data 1 differential
CN3.75	MIPI_DSI_D1_N_IMX7_CONN	DS	Negative DSI data 1 differential

5.1.2 Parallel Display (24 Bits)

The parallel interface of iMX7 can be connected to a parallel display unit up to 24 bits. The numbers of bits per pixel can be configured to 18/24 bit. The eSOMiMX7 also supports ITU-R BT.656 (DVI Mode) mode which allows the RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

The following table lists the parallel display signal details.

Table 7: Parallel Display Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.27	iMX7_LCD_ENABLE	O	Enable signal
CN3.41	iMX7_LCD_VSYNC	O	Display vertical sync
CN3.39	iMX7_LCD_HSYNC	O	Display horizontal sync
CN3.28	CLK_iMX7_LCD_CLK	O	Display pixel clock
CN3.58	iMX7_LCD_RESET	O	Reset signal
CN3.36	iMX7_LCD_DATA0	O	Display data output 0
CN3.54	iMX7_LCD_DATA1	O	Display data output 1
CN3.40	iMX7_LCD_DATA2	O	Display data output 2
CN3.57	iMX7_LCD_DATA3	O	Display data output 3
CN3.38	iMX7_LCD_DATA4	O	Display data output 4
CN3.53	iMX7_LCD_DATA5	O	Display data output 5
CN3.55	iMX7_LCD_DATA6	O	Display data output 6
CN3.35	iMX7_LCD_DATA7	O	Display data output 7
CN3.34	iMX7_LCD_DATA8	O	Display data output 8
CN3.45	iMX7_LCD_DATA9	O	Display data output 9
CN3.49	iMX7_LCD_DATA10	O	Display data output 10
CN3.29	MX7_LCD_DATA11	O	Display data output 11
CN3.32	iMX7_LCD_DATA12	O	Display data output 12
CN3.48	iMX7_LCD_DATA13	O	Display data output 13
CN3.43	iMX7_LCD_DATA14	O	Display data output 14
CN3.42	iMX7_LCD_DATA15	O	Display data output 15
CN3.56	iMX7_LCD_DATA16	O	Display data output 16
CN3.31	iMX7_LCD_DATA17	O	Display data output 17
CN3.46	iMX7_LCD_DATA18	O	Display data output 18
CN3.52	iMX7_LCD_DATA19	O	Display data output 19
CN3.51	iMX7_LCD_DATA20	O	Display data output 20
CN3.50	iMX7_LCD_DATA21	O	Display data output 21

CN3.47	iMX7_LCD_DATA22	O	Display data output 22
CN3.33	iMX7_LCD_DATA23	O	Display data output 23

5.1.3 Electrophoretic Display

eSOMiMX7 has an EPD Controller which is used to interface e-paper displays. It supports resolutions up to 4096 x 4096 pixels with 20 Hz refresh and resolutions up to 1650 x 2332 pixels at 106 Hz refresh.

The following table lists the EPDC signal details.

Table 8: EPDC Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.1	iMX7_CONN_QSPI_A_DATA0	O	EPDC_DATA00
CN3.5	iMX7_CONN_QSPI_A_DATA1	O	EPDC_DATA01
CN3.9	iMX7_CONN_QSPI_A_DATA2	O	EPDC_DATA02
CN3.3	iMX7_CONN_QSPI_A_DATA3	O	EPDC_DATA03
CN3.11	iMX7_CONN_QSPI_A_DQS	O	EPDC_DATA04
CN3.13	iMX7_CONN_QSPI_A_SCLK	O	EPDC_DATA05
CN3.7	iMX7_CONN_QSPI_A_SS0_B	O	EPDC_DATA06
CN3.15	iMX7_CONN_QSPI_A_SS1_B	O	EPDC_DATA07
CN3.2	iMX7_CONN_QSPI_B_DATA0	O	EPDC_DATA08
CN3.8	iMX7_CONN_QSPI_B_DATA1	O	EPDC_DATA09
CN3.10	iMX7_CONN_QSPI_B_DATA2	O	EPDC_DATA10
CN3.14	iMX7_CONN_QSPI_B_DATA3	O	EPDC_DATA11
CN3.6	iMX7_CONN_QSPI_B_DQS	O	EPDC_DATA12
CN3.16	iMX7_CONN_QSPI_B_SCLK	O	EPDC_DATA13
CN3.4	iMX7_CONN_QSPI_B_SS0_B	O	EPDC_DATA14
CN3.12	iMX7_CONN_QSPI_B_SS1_B	O	EPDC_DATA15
CN3.100	P2MDIDN	O	EPDC Source Driver-Chip-enable/Start-Pulse
CN3.98	P2MDIDP	O	EPDC Source Driver-Chip-enable/Start- Pulse
CN3.80	P2MDIBN	O	EPDC Source Driver-Chip-enable/Start-Pulse
CN3.82	P2MDIBP	O	EPDC Source Driver-Chip-enable/Start- Pulse
CN3.18	ETHERNET_P2_ACT	O	EPDC Source Driver-Shift Clock
CN3.20	ETHERNET_P2_LED_1000M	O	EPDC Source Driver-Latch Enable
CN3.22	ETHERNET_P2_LED_100M	O	EPDC Source Driver-Output Enable
CN3.24	CONN_RGMII2_RXD3	O	EPDC Source Driver-Shift direction
CN3.86	P2MDIAP	O	EPDC Gate Driver-Clock
CN3.88	P2MDIAN	O	EPDC Gate Driver-Output Enable
CN3.94	P2MDICN	O	EPDC Gate Driver-Shift direction

CN3.92	P2MDICP	O	EPDC Gate Driver-Start Pulse
CN3.19	iMX7_CONN_EPDC_PWRCOM	O	EPDC Panel-Power control
CN3.21	iMX7_CONN_EPDC_PWRSTAT	O	EPDC Panel-Power status good
CN3.25	iMX7_CONN_EPDC_BDR0	O	EPDC Panel-Border Control
CN3.23	iMX7_CONN_EPDC_BDR1	O	EPDC Panel-Border Control

Note: Electrophoretic display is not a part of eSOMiMX7 Solo.

The EPDC Signals are multiplexed with Ethernet2, so EPDC is not supported in Dual core SOM with Dual Ethernet configuration.

5.2 Camera Subsystem

The camera subsystem consists of the following camera interfaces:

- MIPI CSI
- Parallel Camera (24 bits)

5.2.1 MIPI CSI

The CSI-2 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The following table lists the MIPI CSI signal details.

Table 9: MIPI CSI Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.62	MIPI_CSI_D0_P_IMX7_CONN	DS	Positive CSI-2 data 0 differential
CN3.64	MIPI_CSI_D0_N_IMX7_CONN	DS	Negative CSI-2 data 0 differential
CN3.68	MIPI_CSI_CLK_P_IMX7_CONN	DS	Positive CSI-2 clock differential
CN3.70	MIPI_CSI_CLK_N_IMX7_CONN	DS	Negative CSI-2 clock differential
CN3.74	MIPI_CSI_D1_P_IMX7_CONN	DS	Positive CSI-2 data 1 differential
CN3.76	MIPI_CSI_D1_N_IMX7_CONN	DS	Negative CSI-2 data 1 differential

5.2.2 Parallel Camera (24 bits)

The parallel camera interface of iMX7 can be connected to a parallel display unit up to 24 bits. It provides support for CCIR656 video interface and traditional sensor interface with 8-bit / 16-bit / 24-bit data port for YCbCr, YUV. It also has configurable master clock frequency output to sensor and provides 256 x 64 FIFO to store received image pixel data.

The following table lists the parallel display signal details.

Table 10: Parallel Display Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.31	LCD1_DATA17	I	CSI_DATA00, Data Sensor Signal
CN3.56	LCD1_DATA16	I	CSI_DATA01, Data Sensor Signal
CN3.42	LCD1_DATA15	I	CSI_DATA02, Data Sensor Signal
CN3.43	LCD1_DATA14	I	CSI_DATA03, Data Sensor Signal
CN3.48	LCD1_DATA13	I	CSI_DATA04, Data Sensor Signal
CN3.32	LCD1_DATA12	I	CSI_DATA05, Data Sensor Signal
CN3.29	LCD1_DATA11	I	CSI_DATA06, Data Sensor Signal
CN3.49	LCD1_DATA10	I	CSI_DATA07, Data Sensor Signal
CN3.45	LCD1_DATA09	I	CSI_DATA08, Data Sensor Signal
CN3.34	LCD1_DATA08	I	CSI_DATA09, Data Sensor Signal
CN3.33	LCD1_DATA23	I	CSI_DATA10, Data Sensor Signal
CN3.47	LCD1_DATA22	I	CSI_DATA11, Data Sensor Signal
CN3.50	LCD1_DATA21	I	CSI_DATA12, Data Sensor Signal
CN3.51	LCD1_DATA20	I	CSI_DATA13, Data Sensor Signal
CN3.52	LCD1_DATA19	I	CSI_DATA14, Data Sensor Signal
CN3.46	LCD1_DATA18	I	CSI_DATA15, Data Sensor Signal
CN3.28	LCD1_CLK	I	CSI_DATA16, Data Sensor Signal
CN3.27	LCD1_ENABLE	I	CSI_DATA17, Data Sensor Signal
CN3.39	LCD1_HSYNC	I	CSI_DATA18, Data Sensor Signal
CN3.41	LCD1_VSYNC	I	CSI_DATA19, Data Sensor Signal
CN3.36	LCD1_DATA00	I	CSI_DATA20, Data Sensor Signal
CN3.54	LCD1_DATA01	I	CSI_DATA21, Data Sensor Signal
CN3.40	LCD1_DATA02	I	CSI_DATA22, Data Sensor Signal
CN3.57	LCD1_DATA03	I	CSI_DATA23, Data Sensor Signal
CN3.53	LCD1_DATA05	I	Horizontal Sync (Blank Signal)
CN4.67	I2C3_DATA_IMX7_CONN	I	Horizontal Sync (Blank Signal)
CN3.55	LCD1_DATA06	I	Pixel Clock
CN4.61	I2C4_CLK_IMX7_CONN	I	Pixel Clock
CN3.38	LCD1_DATA04	I	Vertical Sync (Start of Frame)
CN4.69	I2C3_CLK_IMX7_CONN	I	Vertical Sync (Start of Frame)
CN3.35	LCD1_DATA07	O	CMOS Sensor Master Clock
CN4.59	I2C4_DATA_IMX7_CONN	O	CMOS Sensor Master Clock
CN3.58	LCD1_RESET	I	CSI Field Signal

5.3 Gigabit Ethernet

eSOMiMX7 supports two Gigabit Ethernet (1000Base-T) interface port as standard interfaces. The PHY of these interfaces are located on the module. Therefore, an external Gigabit magnetic is required to complete the interface to the media. The module features the AR8035 Integrated 10/100/1000 Gigabit Ethernet Transceiver as PHY which is connected over RGMII with the MAC in the processor. The interface is backward compatible with the 10/100Mbit Ethernet (10/100Base-TX) standard.

The following table lists the 1 Gbps Ethernet1 and Ethernet2 signal details.

Table 11: 1 Gbps Ethernet1 and Ethernet2 Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.97	P1MDIAN	DS	Ethernet1 Negative A differential lane
CN3.99	P1MDIAP	DS	Ethernet1 Positive A differential lane
CN3.85	P1MDIBN	DS	Ethernet1 Negative B differential lane
CN3.87	P1MDIBP	DS	Ethernet1 Positive B differential lane
CN3.91	P1MDICN	DS	Ethernet1 Negative C differential lane
CN3.93	P1MDICP	DS	Ethernet1 Positive C differential lane
CN3.79	P1MDIDN	DS	Ethernet1 Negative D differential lane
CN3.81	P1MDIDP	DS	Ethernet1 Positive D differential lane
CN4.74	ETHERNET_P1_LED_100M	O	Ethernet1 LED Status for 10/100 BASE-T link
CN4.70	ETHERNET_P1_LED_1000M	O	Ethernet1 LED Status for 1000 BASE-T link
CN4.72	ETHERNET_P1_ACT	O	Ethernet1 LED Status for link activity
CN3.88	P2MDIAN	DS	Ethernet2 Negative A differential lane
CN3.86	P2MDIAP	DS	Ethernet2 Positive A differential lane
CN3.80	P2MDIBN	DS	Ethernet2 Negative B differential lane
CN3.82	P2MDIBP	DS	Ethernet2 Positive B differential lane
CN3.94	P2MDICN	DS	Ethernet2 Negative C differential lane
CN3.92	P2MDICP	DS	Ethernet2 Positive C differential lane
CN3.100	P2MDIDN	DS	Ethernet2 Negative D differential lane
CN3.98	P2MDIDP	DS	Ethernet2 Positive D differential lane
CN3.22	ETHERNET_P2_LED_100M	O	Ethernet2 LED Status for 10/100 BASE-T link
CN3.20	ETHERNET_P2_LED_1000M	O	Ethernet2 LED Status for 1000 BASE-T link
CN3.18	ETHERNET_P2_ACT	O	Ethernet2 LED Status for link activity

Note:

- Ethernet2 is not a part of eSOMiMX7 Solo.
- The EPDC signals are multiplexed with Ethernet2, so Ethernet2 is not supported in Dual core SOM with EPDC Configuration.

Based on the presence of pull-up or pull-down on the LED_ACT pin, the physical address of the Ethernet PHY changes. When both the Ethernet are being used then it is necessary that both the Ethernet PHY has separate PHY ID. It is recommended to pull-up LED_ACT pin of Ethernet 1 to 3.3V and pull-down LED_ACT pin of Ethernet 2 so that PHY ID of Ethernet 1 will be 0X04 and PHY ID of Ethernet 2 will be 0X00.

The following table lists the Gigabit Ethernet PHY address details.

Table 12: Gigabit Ethernet PHY Address Details

Configurations	Ethernet 1	Ethernet 2
LED_ACT	Pull-up to 3.3V	Pull-down
PHY ID	0X04	0X00

5.4 Wi-Fi and Bluetooth

eSOMiMX7 contains Wi-Fi and Bluetooth module with the following features:

- IEEE STD 802.11a/b/g/n
- Bluetooth 4.1 and CSA2 Support
- Dual-mode Bluetooth and BLE
- Commercial version (WL1835) is certified for CE (European Conformity) (DoC) and FCC (FCC ID: 2ALXI-SOMWB1)
- Extended Temperature version (WL1837) module is certified for FCC, IC, CE, TELEC.

There are two on-Board UFL Connectors to which an external antenna need to be connected as shown in the following figure

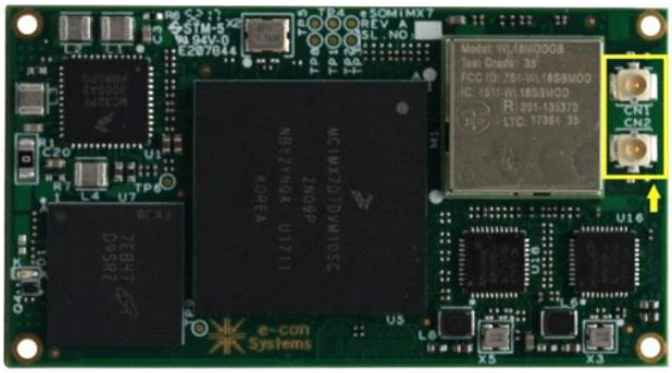

Figure 3: Wi-Fi Antenna Connector

The following table lists the antennas recommended for connecting with two on-Board UFL Connectors.

Table 13: Recommended Antenna

#	Part Number	Manufacturer
1	001-0012 , 080-0013	Laird – Wireless & Thermal solutions
2	CAF94505	Laird Technologies

Note: Please check with e-con Systems before finalizing the Antenna.

5.5 USB 2.0

In this section, you can view the following USB 2.0 interfaces:

- USB 2.0 OTG1
- USB 2.0 OTG2

The following sections describe each of the USB 2.0 interfaces in detail.

5.5.1 USB 2.0 OTG1

eSOMiMX7 contains USB 2.0 OTG1 with the following features:

- High-speed OTG core
- High speed, full speed, and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)

The following table lists the USB 2.0 OTG1 signal details.

Table 134: USB 2.0 OTG1 Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.86	USB_OTG1_DP_iMX7_CONN	DS	Positive USB host data
CN4.88	USB_OTG1_DN_iMX7_CONN	DS	Negative USB host data
CN4.78	USB_OTG1_ID_iMX7_CONN	I	USB host / client identification

5.5.2 USB 2.0 OTG2

eSOMiMX7 contains USB 2.0 OTG2 with the following features:

- High-speed OTG core
- High speed, full speed, and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)

The following table lists the USB 2.0 OTG2 signal details.

Table 15: USB 2.0 OTG2 Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.92	USB_OTG2_DP_iMX7_CONN	DS	Positive USB host data
CN4.94	USB_OTG2_DN_iMX7_CONN	DS	Negative USB host data
CN4.80	USB_OTG2_ID_iMX7_CONN	I	USB host or client identification

Note:

- USB 2.0 OTG2 is a specific feature for eSOMiMX7 Dual interfaces and is not a part of eSOMiMX7 Solo.
- It is recommended to use OTG2 as a Host interface.

5.6 MMC or SD Interface

eSOMiMX7 contains MMC or SD interface with the following features:

- Conforms to the SD Host controller standard specification version 3.0
- Compatible with the MMC system specification version 4.2/4.3/4.4/4.41

The SD cards know different bus speed modes. The required signal voltage depends on the bus speed mode and can be switched between 1.8V and 3.3V as per the mode requirement. It is recommended to use the VCC_SD supply to power the card and for pull-ups used on these lines.

The following table lists the SD interface signal details.

Table 16: SD Interface Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.97	VCC_SD	Power	SD Power Supply railing
CN4.81	CLK_SD1_CLK_iMX7_CONN	O	Clock for MMC/SD/SDIO card
CN4.91	SD1_CMD_iMX7_CONN	IO	CMD line connect to card
CN4.93	SD1_DATA0_iMX7_CONN	IO	DATA0 line
CN4.87	SD1_DATA1_iMX7_CONN	IO	DATA1 line
CN4.89	SD1_DATA2_iMX7_CONN	IO	DATA2 line
CN4.85	SD1_DATA3_iMX7_CONN	IO	DATA3 line
CN4.95	nSD1_CD_iMX7_CONN	I	Card detection pin

5.7 Audio Interface

eSOMiMX7 features two audio interfaces:

- Synchronous Audio Interface
- Medium Quality Sound

5.7.1 Synchronous Audio Interface

eSOMiMX7 has two synchronous audio interface (SAI) interface that can support full-duplex serial interfaces with frame synchronization such as I2S and codec interfaces.

The following table lists the SAI signal details.

Table 147: SAI Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.44	SAI1_TXD_iMX7_CONN	O	Transmit data
CN4.46	SAI1_RXD_iMX7_CONN	I	Receive data
CN4.48	SAI1_TXC_iMX7_CONN	I/O	Transmit Bit Clock
CN4.50	SAI1_RXFS_iMX7_CONN	I/O	Receive Frame Sync
CN4.52	SAI1_RXC_iMX7_CONN	I/O	Receive Bit Clock
CN4.54	SAI1_TXFS_iMX7_CONN	I/O	Transmit Frame Sync
CN4.58	CLK_SAI1_MCLK_iMX7_CONN	I/O	Audio Master Clock
CN4.73	SAI2_RXD_iMX7_CONN	I	Receive Data
CN4.75	SAI2_TXD_iMX7_CONN	O	Transmit data
CN4.77	SAI2_TXC_iMX7_CONN	I/O	Transmit Bit Clock
CN4.71	SAI2_FS_iMX7_CONN	I/O	Transmit Frame Sync
CN4.55	GPIO1_IO02_IMX7_CONN	I/O	Audio Master Clock

Note: SAI1 lines are muxed with NAND signals and hence cannot be used in SOMs with NAND flash.

5.7.2 Medium Quality Sound

Medium quality sound (MQS) is used to generate medium quality audio through a standard GPIO in the pin mux, it accepts 2-channels, LSB-valid 16 bit, MSB shift-out first. It supports 44.1 kHz or 48 kHz bit clock frequency.

The following table lists the MQS signal details.

Table 158: MQS Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.44	SAI1_TXD_iMX7_CONN	O	Transmit data
CN4.46	SAI1_RXD_iMX7_CONN	I	Receive data

5.8 Communication Interface

In this section, you can view the following communication interfaces:

- UART Interface
- FlexCAN Interface
- Serial Peripheral Interface
- I2C interface

The following sections describe each of the communication interfaces in detail.

5.8.1 UART Interface

By default, eSOMiMX7 provides six UART Ports, out of which four has RTS and CTS as hardware flow control along with Rx and Tx lines, while two supports only Rx and Tx lines.

The following table lists the UART signal details.

Table 169: UART Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.68	UART1_TX_IMX7_CONN	O	UART1 Transmitter line
CN4.64	UART1_RX_IMX7_CONN	I	UART1 Receiver line
CN3.27	iMX7_LCD_ENABLE	O	UART2 Transmitter line
CN4.66	UART2_RX_IMX7_CONN	I	UART2 Receiver line
CN3.28	CLK_iMX7_LCD_CLK	I	UART2 Receiver line
CN3.39	iMX7_LCD_HSYNC	I	UART2 Ready to Send line
CN3.41	iMX7_LCD_VSYNC	O	UART2 Clear to Send line
CN4.45	GPIO1_IO09_IMX7_CONN	O	UART3 Transmitter line
CN4.62	UART3_RX_IMX7_CONN	I	UART3 Receiver line
CN4.63	I2C2_DATA_IMX7_CONN	O	UART4 Transmitter line
CN4.77	SAI2_TXC_iMX7_CONN	O	UART4 Transmitter line
CN4.65	I2C2_CLK_IMX7_CONN	I	UART4 Receiver line
CN4.71	SAI2_FS_iMX7_CONN	I	UART4 Receiver line
CN4.75	SAI2_TXD_iMX7_CONN	I	UART4 Ready to Send line

CN4.73	SAI2_RXD_iMX7_CONN	O	UART4 Clear to Send line
CN4.59	I2C4_DATA_IMX7_CONN	O	UART5 Transmitter line
CN4.47	GPIO1_IO07_IMX7_CONN	O	UART5 Transmitter line
CN4.48	SAI1_TXC_iMX7_CONN	O	UART5 Transmitter line
CN4.61	I2C4_CLK_IMX7_CONN	I	UART5 Receiver line
CN4.46	SAI1_RXD_iMX7_CONN	I	UART5 Receiver line
CN4.49	GPIO1_IO06_IMX7_CONN	I	UART5 Receiver line
CN4.67	I2C3_DATA_IMX7_CONN	I	UART5 Ready to Send line
CN4.44	SAI1_TXD_iMX7_CONN	I	UART5 Ready to Send line
CN4.69	I2C3_CLK_IMX7_CONN	O	UART5 Clear to Send line
CN4.51	GPIO1_IO04_IMX7_CONN	O	UART5 Clear to Send line
CN4.54	SAI1_TXFS_iMX7_CONN	O	UART5 Clear to Send line
CN4.87	SD1_DATA1_iMX7_CONN	O	UART7 Transmitter line
CN3.16	iMX7_CONN_QSPI_B_SCLK	O	UART7 Transmitter line
CN4.93	SD1_DATA0_iMX7_CONN	I	UART7 Receiver line
CN3.6	iMX7_CONN_QSPI_B_DQS	I	UART7 Receiver line
CN4.85	SD1_DATA3_iMX7_CONN	I	UART7 Ready to Send line
CN3.4	iMX7_CONN_QSPI_B_SS0_B	I	UART7 Ready to Send line
CN4.89	SD1_DATA2_iMX7_CONN	O	UART7 Clear to Send line
CN3.12	iMX7_CONN_QSPI_B_SS1_B	O	UART7 Clear to Send line

5.8.2 FlexCAN Interface

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol 1.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field such as real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The following table lists the FlexCAN 1 and 2 signal details.

Table 20: FlexCAN 1 and 2 Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.41	GPIO1_IO12_IMX7_CONN	I	CAN1 Bus Receive
CN4.39	GPIO1_IO13_IMX7_CONN	O	CAN1 Bus Transmit
CN4.44	SAI1_TXD_iMX7_CONN	I	CAN2 Bus Receive
CN4.54	SAI1_TXFS_iMX7_CONN	O	CAN2 Bus Transmit

5.8.3 Serial Peripheral Interface

In this section, you can view the following types of SPIs:

- Enhanced Configurable SPI
- Quad SPI

The following sections describe each of the SPIs in detail.

5.8.4 Enhanced Configurable SPI

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO).

The following table lists the enhanced configurable SPI signal details.

Table 171: Enhanced Configurable SPI Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.65	I2C2_CLK_IMX7_CONN	O	SPI1 – SCLK
CN4.73	SAI2_RXD_iMX7_CONN	O	SPI1 – SCLK
CN4.71	SAI2_FS_iMX7_CONN	O	SPI1 – MOSI
CN4.77	SAI2_TXC_iMX7_CONN	I	SPI1 – MOSI
CN4.63	I2C2_DATA_IMX7_CONN	O	SPI1 – SS0
CN4.75	SAI2_TXD_iMX7_CONN	O	SPI1 – SS0
CN4.85	SD1_DATA3_iMX7_CONN	O	SPI1 – SS1
CN3.39	iMX7_LCD_HSYNC	O	SPI2 – SCLK
CN3.28	CLK_iMX7_LCD_CLK	I	SPI2 – MISO
CN4.95	nSD1_CD_iMX7_CONN	I	SPI2 – MISO
CN3.27	iMX7_LCD_ENABLE	O	SPI2 – MOSI
CN3.41	iMX7_LCD_VSYNC	O	SPI2 – SS0
CN4.81	CLK_SD1_CLK_iMX7_CONN	O	SPI2 – SS0
CN4.91	SD1_CMD_iMX7_CONN	O	SPI2 – SS1
CN4.93	SD1_DATA0_iMX7_CONN	O	SPI2 – SS2
CN4.87	SD1_DATA1_iMX7_CONN	O	SPI2 – SS3
CN4.89	SD1_DATA2_iMX7_CONN	I	SPI2 – Ready

5.8.5 Quad SPI

The QSPI acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines. Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.

The following table lists the QSPI signal details.

Table 22: QSPI Signal Details

Pin #	Pin Name	Pin Type	Description
CN3.13	iMX7_CONN_QSPI_A_SCLK	O	QSPI_A_SCLK
CN3.1	iMX7_CONN_QSPI_A_DATA0	IO	QSPI_A_DATA0
CN3.5	iMX7_CONN_QSPI_A_DATA1	IO	QSPI_A_DATA1
CN3.9	iMX7_CONN_QSPI_A_DATA2	IO	QSPI_A_DATA2
CN3.3	iMX7_CONN_QSPI_A_DATA3	IO	QSPI_A_DATA3
CN3.11	iMX7_CONN_QSPI_A_DQS	IO	QSPI_A_DQS
CN3.7	iMX7_CONN_QSPI_A_SS0_B	O	QSPI_A_SS0_B
CN3.15	iMX7_CONN_QSPI_A_SS1_B	O	QSPI_A_SS1_B
CN3.16	iMX7_CONN_QSPI_B_SCLK	O	QSPI_B_SCLK
CN3.2	iMX7_CONN_QSPI_B_DATA0	IO	QSPI_B_DATA0
CN3.8	iMX7_CONN_QSPI_B_DATA1	IO	QSPI_B_DATA1

CN3.10	iMX7_CONN_QSPI_B_DATA2	IO	QSPI_B_DATA2
CN3.14	iMX7_CONN_QSPI_B_DATA3	IO	QSPI_B_DATA3
CN3.6	iMX7_CONN_QSPI_B_DQS	IO	QSPI_B_DQS
CN3.4	iMX7_CONN_QSPI_B_SS0_B	O	QSPI_B_SS0_B
CN3.12	iMX7_CONN_QSPI_B_SS1_B	O	QSPI_B_SS1_B

5.8.6 I2C interface

I2C-1, 2, 3,4 interface connectivity peripherals provide serial interface for the external devices. Data rates of up to 100 kbps are supported.

There are no pull-ups placed internally in eSOMiMX7 and hence requires an external pull-up on the carrier board.

The following table lists the I2C signal details.

Table 183: I2C Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.63	I2C2_DATA_IMX7_CONN	I/O	I2C-2 Serial Data
CN4.47	GPIO1_IO07_IMX7_CONN	I/O	I2C-2 Serial Data
CN4.65	I2C2_CLK_IMX7_CONN	O	I2C-2 Serial Clock
CN4.49	GPIO1_IO06_IMX7_CONN	O	I2C-2 Serial Clock
CN4.66	UART2_RX_IMX7_CONN	O	I2C-2 Serial Clock
CN4.67	I2C3_DATA_IMX7_CONN	I/O	I2C-3 Serial Data
CN3.50	LCD1_DATA21	I/O	I2C-3 Serial Data
CN4.45	GPIO1_IO09_IMX7_CONN	I/O	I2C-3 Serial Data
CN4.69	I2C3_CLK_IMX7_CONN	O	I2C-3 Serial Clock
CN3.51	LCD1_DATA20	O	I2C-3 Serial Clock
CN4.59	I2C4_DATA_IMX7_CONN	I/O	I2C-4 Serial Data
CN4.52	SAI1_RXC_iMX7_CONN	I/O	I2C-4 Serial Data
CN3.33	LCD1_DATA23	I/O	I2C-4 Serial Data
CN4.61	I2C4_CLK_IMX7_CONN	O	I2C-4 Serial Clock
CN4.43	GPIO1_IO10_IMX7_CONN	O	I2C-4 Serial Clock
CN4.50	SAI1_RXFS_iMX7_CONN	O	I2C-4 Serial Clock

CN3.47	LCD1_DATA22	O	I2C-4 Serial Clock

5.9 Miscellaneous

5.9.1 PWM

The Pulse Width Modulation (PWM) has a 16-bit counter.

The following table lists the PWM signal details.

Table 194: PWM Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.53	GPIO1_IO00_IMX7_CONN	O	PWM1 – OUT
CN4.45	GPIO1_IO09_IMX7_CONN	O	PWM2 – OUT
CN4.55	GPIO1_IO02_IMX7_CONN	O	PWM2 – OUT
CN4.43	GPIO1_IO10_IMX7_CONN	O	PWM3 – OUT

5.9.2 Analog Input Signal

eSOMiMX7 has ADC is a 1.8 V,12-bit ADC with 8 analog input mux and level-shifters for low-voltage digital interface. The maximum sample rate of the ADC is 1 MHz.

The following table lists the enhanced configurable SPI signal details.

Table 25: Analog Input Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.28	ADC1_IN0_IMX7_CONN	I	Analog input
CN4.32	ADC1_IN1_IMX7_CONN	I	Analog input
CN4.26	ADC1_IN2_IMX7_CONN	I	Analog input
CN4.30	ADC1_IN3_IMX7_CONN	I	Analog input
CN4.34	ADC2_IN0_IMX7_CONN	I	Analog input
CN4.36	ADC2_IN1_IMX7_CONN	I	Analog input
CN4.38	ADC2_IN2_IMX7_CONN	I	Analog input
CN4.40	ADC2_IN3_IMX7_CONN	I	Analog input

5.10 PCIe Interface

The PCIe 2.1 PHY supports both the 6 Gbps data rate of the PCI Express Gen 2.1 specifications.

The following table lists the PCIe signal details.

Table 26: PCIe Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.28	ADC1_IN0_IMX7_CONN	I	Analog input
CN4.32	ADC1_IN1_IMX7_CONN	I	Analog input
CN4.26	ADC1_IN2_IMX7_CONN	I	Analog input
CN4.30	ADC1_IN3_IMX7_CONN	I	Analog input
CN4.34	ADC2_IN0_IMX7_CONN	I	Analog input
CN4.36	ADC2_IN1_IMX7_CONN	I	Analog input
CN4.38	ADC2_IN2_IMX7_CONN	I	Analog input
CN4.40	ADC2_IN3_IMX7_CONN	I	Analog input

Note: PCIe is a specific feature for eSOMiMX7 Dual interfaces and is not a part of eSOMiMX7 Solo interfaces.

5.11 CPU Control Signals

The CPU control signals can be used for controlling the boot flow mode and power mode of the CPU.

The following table lists the CPU control signal details.

Table 27: CPU Control Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.99	BASE_BOARD_PWR_EN	O	Carrier board power enable signal.
CN4.37	CPU_BOOT_MODE0	I	Boot Mode Configuration Pin 1. Please refer to the Boot options section for more information.
CN4.35	CPU_BOOT_MODE1	I	Boot Mode Configuration Pin 2. Please refer to the Boot options section, for more information.
CN4.31	CPU_ONOFF	I	CPU Power on Switch. Please refer to the CPU Power and Reset section, for more information.
CN4.33	CPU_POR	I	CPU Reset. Please refer to the CPU Power and Reset section, for more information.

5.11.1 CPU Reset

The reset circuit is recommended to perform a software initiated reset or to perform a watchdog initiated reset. In the case of watchdog reset, the GPIO1_IO00_IMX7_CONN must be used under ALT3_WDOG1_WDOG_B mux option to control POR.

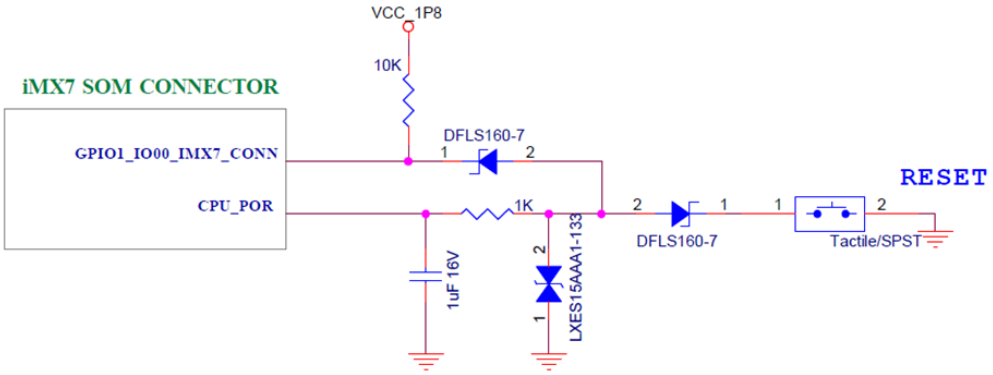

Figure 4: Reset Circuit Reference Schematic Diagram

5.11.2 Power on Sequence

The power on sequence begins with the VCC_3P3_IN supply to the SOM, this is the first and foremost supply given to the SOM. After the completion of internal power on sequence in the SOM, the BASE_BOARD_PWR_EN signal is pulled high. Only after this, the baseboard is powered ON. It is mandatory to follow this sequence to ensure the proper working of all the peripherals.

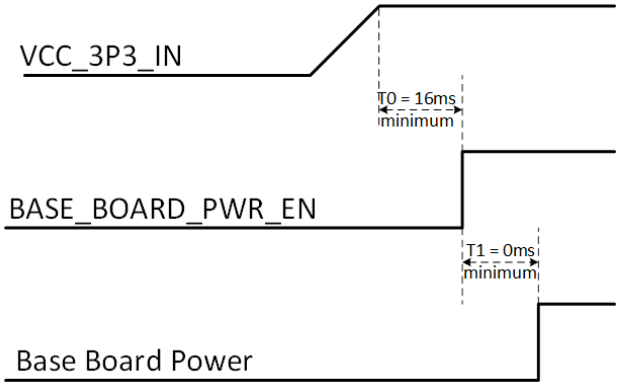

Figure 5: Power on Sequence

5.11.3 Wake-up Source

The wake-up signals can be used to wake up the processor from the deep sleep mode to its normal state.

The following table lists the wake-up signal details.

Table 28: Wake-up Signal Details

Pin #	Pin Name	Pin Type	Description
CN4.31	CPU_ONOFF	SNVS	Internally pulled up to SNVS Voltage.
CN4.39	GPIO1_IO13_IMX7_CONN	1.8V	
CN4.41	GPIO1_IO12_IMX7_CONN	1.8V	
CN4.43	GPIO1_IO10_IMX7_CONN	1.8V	
CN4.45	GPIO1_IO09_IMX7_CONN	1.8V	
CN4.47	GPIO1_IO07_IMX7_CONN	1.8V	

CN4.49	GPIO1_IO06_IMX7_CONN	1.8V	
CN4.51	GPIO1_IO04_IMX7_CONN	1.8V	
CN4.53	GPIO1_IO00_IMX7_CONN	1.8V	

Note: The wake up can also be performed by using the internal real time clock (RTC).

This section describes the various boot options and includes the electrical specification of eSOMiMX7.

6 Boot options

eSOMiMX7 SOM uses two boot mode signals to select the boot type.

The following table lists the boot mode type selection details.

Table 209: Boot Mode Type Selection

Boot Mode	Description	BOOT_MODE1	BOOT_MODE0
Boot From eFuses	In this mode, i.MX7 boot media is selected by GPIO eFUSE settings	0	0
Serial Downloader Mode	In this mode, i.MX7 boot device can be programmed through its USB OTG interface using MFG Tool	0	1
Internal Boot Mode (Default)	In this mode, i.MX7 boot media is selected by GPIO Pin's settings	1	0
Reserved	Not allowed to use this mode	1	1

Note:

- 1 – Pin need to be connected to logic high.
- 0 – Pin need to be connected to logic low.

6.1 CPU Power and Reset

eSOMiMX7 supports external control signals to control the power flow of CPU.

The following table lists the CPU power and reset details.

Table 30: CPU Power and Reset

Signal	Description
CPU_POWER_ON	CPU Reset signal is used to switch on and off the system. Can be connected to a push button. If not used, set CPU reset signal to logic level high.
CPU_RESET	CPU Reset signal is used to reset the processor and begin the boot flow by reading the values of the boot mode select pins.

7 Electrical Specification

The electrical specification of eSOMiMX7 includes the following:

- Power Supply and Ground Pins
- Power Supply Input
- DC Electrical Characteristics
- Environmental Specifications

7.1 Power Supply and Ground Pins

The following table lists the power supply and ground pins details.

Table 31: Power Supply and Ground Pins

Pin #	Pin Name	Pin Type	Description
CN4.2,4,6,8,10,12,14,16,18,20,22	VCC_3P3_IN	P	3.3V Supply to the SOM must be provided from the carrier board.
CN4.1	VCC_LICELL	P	Coin cell supply input/output. Bypass with 0.1 µF capacitor. Connect to optional coin cell.
CN4.76	VBUS_USB_OTG1	P	VBUS input for USB_OTG1.
CN4.92	VBUS_USB_OTG2	P	VBUS input for USB_OTG2.
CN4.29	VDD_SNVS_1P8_CAP	P	SNVS Regulated output.
CN4.97	VCC_SD	P	Supply for SD card generated from SOM Internally for various power modes.
CN3.17,26,30,37,44,59,60,65,66,71,72,77,78,83,84,89,90,95,96 CN4.3,9,15,21,24,42,56,57,60,79,83,84,90,96	GND	P	Digital ground.

7.2 Power Supply Input

Main Power Supply: 3.3V Tolerance Allowed: +/- 5%

Table 212: Current consumption table

S .No	Test Case	Current (mA)
1	Peak current consumption during boot up	370
2	Current consumption after the OS has booted	215
3	Current consumption with video streaming in MIPI DSI Ethernet-1 Iperf test @ 100Mbps,	450

	Sample file copy in both OTG, Sample file copy in SD Sample file copy in eMMC audio playing	
4	Current consumption with video streaming in HDMI Ethernet-1 Iperf test @ 100Mbps, Sample file copy in both OTG, Sample file copy in SD Sample file copy in eMMC audio playing	470
5	Current During DEEP Sleep	3

Note:

Current consumption varies depending upon the use case.

All the above measurements are taken in eSOMiMX7-CD -F4G-R1G -WB-DE SOMs

7.3 DC Electrical Characteristics

Note: OVDD is the IO signal voltage level (1.8V or 3.3V).

The following table lists the DC electrical characteristics.

Table 223: DC Electrical Characteristics

Use case	Min	Type	Max	Units
High-level output voltage	V_{oh}	0.8 x OVDD	OVDD	Volts
Low-level output voltage	V_{ol}	0	0.2 x OVDD	Volts
High-Level DC input voltage	V_{ih}	0.7 x OVDD	OVDD + 0.3	Volts
Low-Level DC input voltage	V_{il}	-0.3	0.3 x OVDD	Volts

7.4 Environmental Specifications

The following table lists the thermal characteristics.

Table 34: Thermal Characteristics

Use case	Min	Type	Max	Units
High-level output voltage	V_{oh}	0.8 x OVDD	OVDD	Volts
Low-level output voltage	V_{ol}	0	0.2 x OVDD	Volts
High-Level DC input voltage	V_{ih}	0.7 x OVDD	OVDD + 0.3	Volts
Low-Level DC input voltage	V_{il}	-0.3	0.3 x OVDD	Volts

This section includes the mechanical drawing and mounting-hole position and dimension of the eSOMiMX7.

8 Mounting-Hole Position and SOM Dimension

The mechanical drawing and mounting-hole position and dimension of the eSOMiMX7 are shown in the following figures.

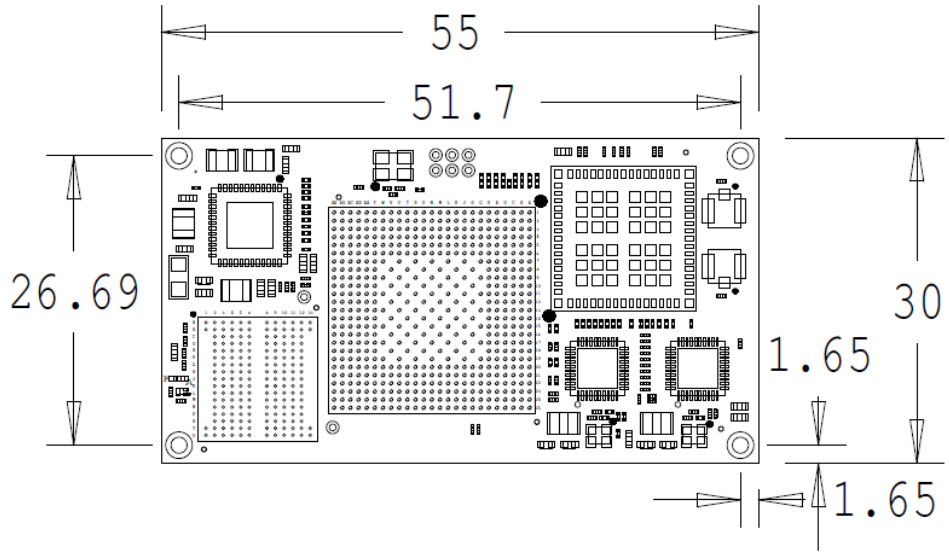

Figure 6: SOM Mechanical Specification Top View

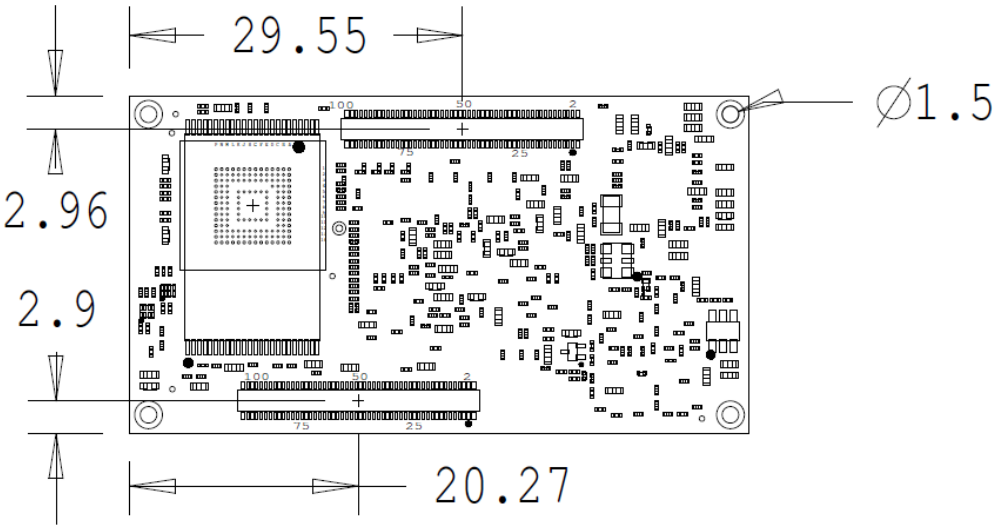

Figure 7: SOM Mechanical Specification Bottom View

Note: All dimensions are in mm.

Glossary

CAN: Controller Area Network.

CPU: Central Processing Unit.

CSI: Camera Sensor Interface.

DSI: Display Sensor Interface.

ECSPI: Enhanced Configurable Serial Peripheral Interface.

eMMC: Embedded Multimedia Card.

MIPI: Mobile Industry Processor Interface.

MMC: Multimedia Card.

PCIe: Peripheral Component Interconnect Express.

PWM: Pulse Width Modulation.

QSPI: Quad SPI.

RTC: Real Time Clock.

UART: Universal Asynchronous Receiver Transmitter.

USB: Universal Serial Bus.

USB 2.0: Universal Serial Bus High speed.

Support

Contact Us

If you need any support on eSOMiMX7 product, please contact us using the Live Chat option available on our website - https://www.e-consystems.com/

Creating a Ticket

If you need to create a ticket for any type of issue, please visit the ticketing page on our website - https://www.e-consystems.com/create-ticket.asp

RMA

To know about our Return Material Authorization (RMA) policy, please visit the RMA Policy page on our website - https://www.e-consystems.com/RMA-Policy.asp

General Product Warranty Terms

To know about our General Product Warranty Terms, please visit the General Warranty Terms page on our website - https://www.e-consystems.com/warranty.asp

Revision History

Rev	Date	Description	Author
1.0	09 Feb 2018	Initial draft version	Ajay Arul
1.1	07 Mar 2018	Ordering Information updated EPDC Signal Description updated	Ajay Arul
1.2	26 APR 2018	Ordering Information updated Voltage Domain Change for some GPIO pins	Ajay Arul
1.3	08 MAY 2018	Wi-Fi certification details updated Wake up details added	Ajay Arul